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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,269	05/25/2001	Sasan Cyrusian	10808/27	5524

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EXAMINER	
COX, CASSANDRA F	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/866,269	CYRUSIAN, SASAN	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's arguments filed 02/24/03 have been fully considered but they are not persuasive. The rejection with respect to claims 1, 4, and 6 have been repeated below.

2. Applicant's arguments with respect to claims 7, 10, 13-16, and 19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claims 16 and 17 are objected to because of the following informalities: Claims 16 and 17 are objected to because they depend from previously cancelled claim 15. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-14 and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Du (U.S. Patent No. 5,638,030).

In reference to claim 1, Du discloses in Figure 15 a differential controlled delay unit (4500'-1), comprising: a first amplifier (4910, 4920) having a first and second transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor (4910) is connected to a drain of the second transistor (4920) and a gate of the second transistor (4920) is connected to a drain of the first transistor (4910); and a second amplifier (4930, 4940) having a third and fourth transistor, a drain of the third and fourth transistors connected to a drain of the first and second transistors to form

output terminals (no-1, po-1), wherein a differential input voltage (pi-1, ni-1) is connected to gates of the second amplifier transistors (4930, 4940), and a control input and power supply voltage (Vcnt', Vdd) is connected to sources of the first amplifier (4910, 4920).

In reference to claim 2, Du also discloses in Figure 15 that the first amplifier transistors (4910, 4920) are PMOS transistors and the second amplifier transistors (4930, 4940) are NMOS transistors.

In reference to claim 3, Du also discloses in Figure 15 that a positive supply voltage (Vcnt', Vdd) is connected to the first amplifier (4910, 4920) and a negative supply voltage (Gnd) is connected to the second amplifier (4930, 4940).

In reference to claim 4, Du discloses in Figure 13 a differential controlled delay unit (4500-1), comprising: a first amplifier (5930, 5940) having a first and second transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor (5930) is connected to a drain of the second transistor (5940) and a gate of the second transistor (5940) is connected to a drain of the first transistor (5930); and a second amplifier (5910, 5920) having a third and fourth transistor, a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals (po-1, no-1), wherein a differential input voltage (ni-1, pi-1) is connected to gates of the second amplifier transistors (5910, 5920), and a control input and power supply voltage (Vcnt', Vdd) is connected to sources of the second amplifier (5910, 5920).

In reference to claim 5, Du also discloses in Figure 13 that the first amplifier transistors (5930, 5940) are NMOS transistors and the second amplifier transistors (5910, 5920) are PMOS transistors.

In reference to claim 6, Du also discloses in Figure 13 that a positive supply voltage (Vcnt', Vdd) is connected to the second amplifier (5910, 5920) and a negative supply voltage (Gnd) is connected to the first amplifier (5930, 5940).

In reference to claim 7, Du discloses in Figure 12 a voltage controlled oscillator (2000'), comprising: a first delay unit (4500-1) and a second delay unit (4500-2), each further comprised of four transistors (see Figure 15), the delay units (4500-1, 4500-2) each having a first amplifier (4910, 4920) having a first and second transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor (4910) is connected to a drain of the second transistor (4920) and a gate of the second transistor (4920) is connected to a drain of the first transistor (4910), the delay units (4500-1, 4500-2) each having a second amplifier (4930, 4940) having a third and fourth transistor, wherein a drain of the third and fourth transistors is connected to a drain of the first and second transistors, the connections forming output terminals (no-1, po-1, no-2, po-2) of the delay unit, and wherein output terminals of the first delay unit (4500-1) are connected to gates of the second amplifier of the second delay unit (4500-2), and output terminals of the second delay unit (4500-2) are connected to gates of the second amplifier of the first delay unit (4500-1), this is seen to be true when the oscillator consists of two delay units, and wherein a control input and power supply voltage (Vcnt', Vdd) is connected to sources of the first amplifiers (4910, 4920).

In reference to claim 8, Du also discloses in Figure 15 that the first amplifier transistors (4910, 4920) are PMOS transistors and the second amplifier transistors (4930, 4940) are NMOS transistors. The same applies to claims 11, 13, and 17.

In reference to claim 9, Du also discloses in Figure 15 that a positive supply voltage (Vcnt', Vdd) is connected to the first amplifier (4910, 4920) and a negative supply voltage (Gnd) is connected to the second amplifier (4930, 4940).

In reference to claim 10, Du discloses in Figure 12 the oscillator (2000') comprising an additional delay unit (4500-k). The same applies to claims 12, 14, 16, and 19, wherein output terminals of a delay unit (4500-1 to 4500 1-K) are connected to gates of a next delay unit (4500-2 to 4500-K), and output terminals of a last delay unit (4500-K) are connected to the gates of the first delay unit (4500-1).

In reference to claim 18, Du discloses in Figure 2 a charge pump (160) and a buffer (560-1, shown in Figure 12), wherein a buffered output voltage (Vcnt') of the charge pump (160) is a supply voltage to the first amplifiers (4910, 4920 of Figure 15).

> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1, 4, and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Proebsting (U.S. Patent No. 6,154,064).

In reference to claim 1, Proebsting discloses in Figure 1 a circuit comprising: a first amplifier having a first (16) and second (17) transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor (16) is connected to a drain of the

second transistor (17) and a gate of the second transistor (17) is connected to a drain of the first transistor (16); and a second amplifier having a third (14) and fourth (15) transistor, a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals (OUT1, OUT2), wherein a differential input voltage (IN1, IN2) is connected to gates of the second amplifier transistors, and a control input and power supply voltage (40 through transistor 28) is connected to sources of the first amplifier. The same applies to claim 4, wherein a control input and supply voltage (30) is connected to the sources of the second amplifier.

In reference to claim 6, a positive supply voltage (30) is connected to the second amplifier and a negative supply voltage is connected to the first amplifier (40 through transistor MP8).

7. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Mizuno (U.S. Patent No. 6,414,556).

In reference to claim 1, Mizuno discloses in Figure 4 a differential controlled delay unit (102), comprising: a first amplifier (MP_{35}, MP_{36}) having a first and second transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor (MP_{35}) is connected to a drain of the second transistor (MP_{36}) and a gate of the second transistor (MP_{36}) is connected to a drain of the first transistor (MP_{35}); and a second amplifier (MN_{33}, MN_{34}) having a third and fourth transistor, a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals (while only a terminal 203 is shown it is well known by one skilled in the art that the differential output would be generated at the gate node of the first transistor MP_{35}), wherein a differential input voltage is connected to gates of the second amplifier

transistors (MN_{33}, MN_{34}), and a control input and power supply voltage (206) is connected to sources of the first amplifier (MP_{35}, MP_{36}). The same applies to claim 4, wherein a control input and supply voltage (207) is connected to the sources of the second amplifier (MN_{33}, MN_{34}).

In reference to claim 2, Mizuno also discloses in Figure 4 that the first amplifier transistors (MP_{35}, MP_{36}) are PMOS transistors and the second amplifier transistors (MN_{33}, MN_{34}) are NMOS transistors.

In reference to claim 3, Mizuno also discloses in Figure 4 that a positive supply voltage (206) is connected to the first amplifier (MP_{35}, MP_{36}) and a negative supply voltage (207) is connected to the second amplifier (MN_{33}, MN_{34}), see column 8, lines 32-36.

Response to Arguments

8. Applicant's arguments filed 02/24/03 with respect to the element 28 have been fully considered but they are not persuasive. There is no language in the claims that would exclude the delay unit from having additional elements. The circuit of Proebsting has all of the required elements of the claims. Therefore, the rejection with respect to claims 1, 4, and 6 has been repeated.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-5735. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM and on alternate Fridays from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

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April 29, 2003

/TIMOTHY P. CALLAHAN
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